PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of: Attorney Docket No.: 3020.02US02

Steven J. Meyer

Application No.: 09/899,763

Filed: July 5, 2001 Group Art Unit: 2123

For: DIGITAL AND ANALOG MIXED SIGNAL SIMULATION USING PLI API

PETITION TO MAKE APPLICATION SPECIAL
UNDER 37 C.F.R. §1.102(d)

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Applicant hereby petitions to make the above-identified and enclosed non-provisional patent application special under 37 C.F.R. §1.102(d) and per the requirements of MPEP 708.02, paragraph VIII (Accelerated Examination). The petition fee of $130.00 required under 37 C.F.R. §1.17(h) is enclosed herewith.

Applicant submits that the prerequisites for making the application special have been met, per MPEP 708.02, paragraph VIII, in that: (1) the enclosed application includes claims directed to a single invention, or in the case the Examiner finds that the claims define more than one invention, Applicant agrees to make an election without traverse; (2) a pre-examination search was performed within United States patents and foreign patents in *U.S. Classes/subclasses 703/014, 013, 002, 015, 016, 003, 017; 708/003; 714/726; 716/001, 004, 005, 006, 018, 019*; (3) one copy of each of the references deemed most closely related to the subject matter

encompassed by the claims is enclosed; and (4) a detailed discussion of the references and how the claimed subject matter is patentable over the references is provided below.

Discussion of the References

The references that are enclosed and discussed below consist of:

U.S. Patent No.	Inventors
5,471,409	Tani
5,297,066	Mayes
5,105,373	Rumsey et al.
5,991,522	Shoen
4,985,860	Vlach
5,394,346	Milsom
4,792,913	Buckland et al.
5,481,484	Ogawa et al.
5,822,567	Takeuchi
6,110,217	Kazmierski et al.

U.S. Patent No. 5,471,409, entitled "Logic Simulation Apparatus and Circuit Simulation Apparatus" describes a system wherein the circuit simulator is used to determine propagation delay times that are then input to the logic simulator. The logic simulator, which has been programmed with circuit connection data, uses the propagation delay times to simulate a circuit. The apparatus of the '409 patent provides no true mixed simulation as information is not transferred back and forth between the two simulators but rather is only uni-way directional. The present invention enables the transfer of information back and forth between the analog simulator and digital simulator for true mixed signal simulation.

U.S. Patent No. 5,297,066, entitled "Digital Circuit Simulation of Analog/Digital Circuits" describes a system wherein analog components are simulated through use of a cell

library that defines analog components in digital terms. Analog values are represented as digital bit vectors giving all possible voltage levels. The method described within the '066 patent is limited to simplified analog models because analog circuit equations are not solved. The present invention is able to address complex analog circuits through use of an analog simulation engine that simulates analog components by solving circuit description differential equations.

U.S. Patent No. 5,105,373, entitled "Method of Simulating the Operation of a Circuit Having Analog and Digital Circuit Parts" describes a method wherein the analog portion of a circuit is simulated by using separate computer code (functions). These functions are called by the digital simulator. The '373 method models analog components by using either tables or transfer functions rather than analog circuit equations resulting in an inaccurate analog model. The present invention models analog circuits through use of an analog simulation engine that simulates analog components by solving circuit description differential equations to provide a very accurate model of the analog circuit.

U.S. Patent No. 5,991,522 entitled "Method and Apparatus for Circuit Conversion for Simulation, Simulator Using Same and Computer-Readable Medium with a Program Therefor Stored Thereon" describes a method/apparatus wherein analog components are converted to a circuit that is suitable for digital simulation only. The present invention provides for the combination of both analog and digital simulation.

U.S. Patent No. 4,985,860 entitled "Mixed-Mode-Simulator Interface" describes a method wherein analog waveforms are synchronized with digital time, the digital time rolling back analog time when needed. The description of the method makes the presumption of an

existing system simulator with analog and digital domains and, as such, discusses only the synchronization of time.

U.S. Patent No. 5,394,346 entitled "Simulation of an Electronic System Including Analog and Digital Circuitry Using High Level Macro Models" describes a method of single kernel simulation wherein analog elements are modeled by high level analog macros and digital elements are modeled by high level digital macros. The macros are constructed by extracting circuit layout data and converting that data to tables or analog transfer functions. The analog circuits are simulated using inaccurate repeated approximations. Circuit properties are repeatedly extracted and used as inputs for other high level macros for which repeated approximations are made. The results of the approximations are then used to re-extract circuit properties. Note that the '346 does not describe mixed signal simulation. The present invention does not utilize repeated approximation but rather differential equations to provide an accurate model of an analog circuit. The present invention additionally provides for mixed signal simulation.

U.S. Patent No. 4,792,913 entitled "Simulator For Systems Having Analog and Digital Portions" describes a method wherein data extraction and file sharing are used to communicate analog node values to a digital simulator, and to communicate digital signal values to an analog simulator. However, the data transfer and synchronization is determined during simulator implementation. As such, data transfer and synchronization cannot be coded by the user or dynamically changed using earlier simulation results. The present invention enables changes to be implemented during simulation.

U.S. Patent No. 5,481,484 entitled "Mixed Mode Simulation Method and Simulator" describes a system wherein digital and analog simulations are executed alternately. In this system the digital analyzed circuit portion current usage is extracted and used by the analog simulator to improve the accuracy of analog simulation. There is a control program that synchronizes time in the digital analyzed portion by reading analog port computed information. The method can be described as a single kernel type mixed mode but not as a mixed signal simulator that is specialized to use digital current to improve the analog circuit simulation accuracy. Data exchange is oblivious in that the digital portion calculates current usage that is read by the analog engine when it needs it and the analog portion calculates time synchronization points that are read by the digital portion. In this system, data transfer and synchronization is determined during simulator implementation preventing the ability of data transfer and synchronization to be coded by the user or dynamically chanted using earlier simulation results, which are features the present invention provides. Also, the method does not address interfaces between analog and digital parts of one mixed signal IC so it is not suitable for mixed simulation of mixed signal designs.

U.S. Patent No. 5,822,567 entitled "Method of and Apparatus for Simulating Integrated Circuit" describes a system wherein separate parts of digital and analog simulation are sped up through the use of a controller that operates to determine when analog simulation can be avoided, i.e., the time to simulate is reduced if certain analog simulation is not performed. However, this system does not enable data exchange, rather, the analog and digital simulators are only interleaved through use of the controller. The present invention provides for data exchange while also providing for enhanced speed of simulation.

U.S. Patent No. 6,110,217, entitled "System and Method for Synchronization of Multiple Analog Servers on a Simulation Backplane" describes a system wherein multiple analog simulators, simulating different portions of a circuit, communicate through a simulation backplane by using block waveform relaxation. The '217 patent addresses only analog simulation. It describes an analog only simulation method that does not address the issue of simulating mixed signal designs.

As to the claimed invention, none of the above-cited patents discloses a system for simulating a circuit that has both analog and digital component, the circuit having been coded into a hardware description language, wherein the system provides the following combination of elements: (1) a digital simulator that uses a programming language interface; (2) an analog simulator that uses the same programming language interface; and (3) a mixed signal program that, once again, uses the same programming language interface to not only control the digital and analog simulator but to also synchronize digital and analog time.

The claimed configuration for a system and method provides for a digital simulation engine that performs discrete digital event simulation and an analog simulation engine that simulates analog components by solving circuit description differential equations, as well as a mixed signal program that acts as an interface between the other engines by reading data, writing data, scheduling changes, monitoring for changes and coordinating discrete digital time with continuous analog time.

Because programming language interfaces (PLIs) are defined for all modern hardware description languages (HDLs), the mixed signal program comprises computer code that functions by making calls to the various programming language interface's (PLIs) application

programming interface (API) library routines. The present invention makes use of standardized APIs for HDLs that allow user application specific computer procedures to be linked with simulation computer program object code to produce application specific enhanced simulation programs. Use of PLIs by the present invention allow mixed signal functionality (mixed signal engine) to be developed separately from simulation program development. PLIs are also commonly available and usually standardized so that simulators can be mixed and matched depending on choice of brands of digital and analog simulators. Yet, using well understood computer program and library linking, the result of development is still one computer program that implements the AMS simulation invention.

The system and method of the present invention allows independent development and selection of both digital event and analog circuit simulators. The present invention may be embodied by using legacy simulators for simulating various analog and digital circuit descriptions coded in analog and digital HDLs. An embodiment which simulates circuits described with net lists and transistor interconnections using the most popular HDLs would combine the digital simulation engine for the Verilog digital HDL with the Spice analog HDL. The present invention's preferred embodiment uses new unified syntax, standardized AMS languages such as Verilog-AMS where both analog and digital circuits are coded in the same HDL. These unified languages have the advantage of allowing user definition of and automatic insertion of mixed signal interfaces.

Within the present invention, PLI routines are called by the mixed signal program to allow discrete digital values to be converted to continuous analog node values for use in analog simulation (called AtoD conversion) and to convert continuous analog node values to discrete

digital logic values (called DtoA conversion) for use in digital simulation. The present invention is used to verify not only analog and digital circuit function but also to accurately model and verify increasingly more common interactions between analog and digital system components required for accurately modeling mixed signal communication ICs. The present invention also allows AMS simulation where analog simulation uses non-standard circuit properties such as frequency domain simulation of high frequency wireless circuits.

The present invention that is disclosed herein provides advantages over the two most popular current mixed signal simulation methods. With respect to the unified kernel approach, the present invention provides the advantage of allowing the use of off the shelf digital and analog simulators while preserving the fine granularity of a unified kernel. With respect to disjoint or decoupled simulation with data exchange, the present invention provides the advantage of tightly coupled simulation using standardized PLI APIs.

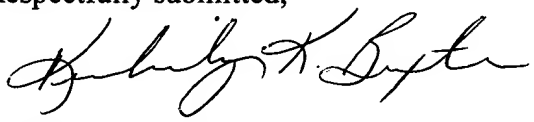
The present invention allows efficient simulation because the HDL PLIs it uses have been designed for efficiency, although in most cases, the mixed signal efficiency is overshadowed by the time required to solve analog differential equations. An additional advantage of the present invention is that the same HDL PLIs used to construct the invention can be utilized by the user of the invention to add other simulation functionality. Examples of possible added user PLI functionality are: user PLI programming to monitor AtoD converter voltage margins during AMS simulation, or user PLI programming to model, at an abstract functional level, digital components for which detailed design is not yet completed.

The present invention is general purpose because it works with any HDL, and any digital simulator brand of the HDL. In addition, it works with any equation solving method used by

analog simulators (usually called solver engines). The present invention provides the most advantages when the one or more HDLs and their associated PLIs are standardized (as is now common practice usually as an IEEE and/or ISO standard) so that many different simulator brands are available in the market. In the invention's preferred embodiment, one combined AMS HDL is used that allows mixed signal interfaces to be coded by users inside the HDL and allows one unified instance tree to be coded.

In view of the above, Applicant respectfully submits the prerequisites for accelerated examination, per MPEP 708.02, paragraph VIII (Accelerated Examination), have been met and that the requirements for making the present application special per 37 C.F.R. § 1.102(d) have been met. As such, Applicant requests that the Commissioner grant the petition and move the application forward for accelerated examination.

Respectfully submitted,



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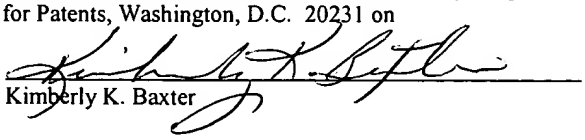

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